

WHAT IS CLAIMED IS:

1. A memory control device comprising:

a memory controller for controlling an
operation of a DRAM and for outputting a clock enable
5 signal to said DRAM;

a power controller for controlling supplying of
power to said DRAM from a main power supply or a
back-up battery power supply and for detecting power
stoppage of said main power supply; and

10 pull-down resistance for pulling down the clock
enable signal to low level; and wherein

if said power controller detects the power
stoppage of said main power supply during a normal
operation, said power controller switches a power
15 supply for said DRAM from said main power supply to
said battery power supply and instructs a self-
refresh mode to said memory controller, so that said
memory controller changes the clock enable signal for
said DRAM to the low level to establish the self-
20 refresh mode of said DRAM, and

after said DRAM is set to the self-refresh mode,
the supplying of power to said memory controller is
stopped, and, even after the stoppage, the clock
enable signal is maintained to the low level by said
25 pull-down resistance, thereby maintaining the self-
refresh mode.

2. A memory control device according to claim 1,
wherein, if said power controller detects the power
stoppage of said main power supply during the normal
operation, said power controller switches a power
5 supply for said memory controller from said main
power supply to said battery power supply, and, after
the self-refresh mode of said DRAM is established by
said memory controller, the supplying of power to
said memory controller from said battery power supply
10 is stopped.

3. A memory control device according to claim 2,
wherein the supplying of power to said memory
controller from said battery power supply is stopped
15 by switching the power supply for said memory
controller from said battery power supply to the
stopped main power supply.

4. A memory control device according to claim 3,
20 wherein, when said memory controller informs said
power controller of the fact that the self-refresh
mode of said DRAM is established, said power
controller stops the supplying of power to said
memory controller from said battery power supply.

25

5. A memory control device according to claim 1,
wherein power is supplied to said memory controller

only by said main power supply, and, if the power
stoppage of said main power supply occurs during the
normal operation, the power is supplied to said
memory controller from said main power supply until
5 the self-refresh mode of said DRAM is established by
said memory controller.

6. A memory control device according to claim 1,
wherein, if said power controller detects the power
10 stoppage of said main power supply during the normal
operation, said power controller instructs the self-
refresh mode by changing an instruction signal for
instructing the self-refresh mode to said memory
controller to active.

15

7. A memory control device according to claim 1,
wherein, if said power controller detects the power
stoppage of said main power supply during the normal
operation, said power controller maintains an
20 instruction signal for the self-refresh mode to
active until immediately after said main power supply
is restored and system reset is cancelled after the
instruction signal was made active, and

said memory controller maintains the clock
25 enable signal to the low level while the instruction
signal is being active upon restoring of said main
power supply, thereby maintaining the self-refresh

mode of said DRAM.

8. A memory control device according to claim 1,
wherein, when said main power supply is normally
5 being ON, after system reset is cancelled, said
memory controller executes power-on initial sequence
for said DRAM to establish the normal operation, and
when said main power supply is restored after
the power stoppage, after the system reset is
10 cancelled, Auto-Refresh Command is issued without
executing the power-on initial sequence for said DRAM,
thereby entering into the normal operation.

9. A memory control device according to claim 8,
15 wherein said power controller makes an instruction
signal for the self-refresh mode inactive when said
main power supply is normally being ON and maintains
the instruction signal to active until immediately
after the system reset is cancelled upon restoring of
20 said main power supply after the power stoppage, and
when the system reset is cancelled, said memory
controller determines whether or not the power-on
initial sequence for said DRAM in accordance with the
fact whether the instruction signal is active or not.

25

10. A memory control device according to claim
1, wherein said power controller monitors voltage of

said main power supply so that, if the voltage is reduced below a predetermined value, the power stoppage is detected.